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E/W-Band GaN MMICs for RF Sensing and Wireless Communication

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Summary

This abstract describes the results of some E/W-band front-end circuits manufactured in a 60 nm GaN-on-silicon process. Firstly, a wideband (~70-95 GHz) LNA and a resistive down-conversion mixer with a frequency doubler were integrated in a W-band 60 nm GaN-on-Si single-chip receiver for the first time. Secondly, an up-converter circuit realised in the same process results in the lowest conversion loss and smallest chip area among GaN mixers at E/W-band. Thirdly, a 6-stage driver has an attractive combination of small size together with a relatively high measured gain and output power in a wide bandwidth. The front-end MMICs can be more area-efficient options for GaN-on-Si E/W-band single-chip transceivers and active phased arrays due to theirs compact sizes and comparably high performance in a broad bandwidth.

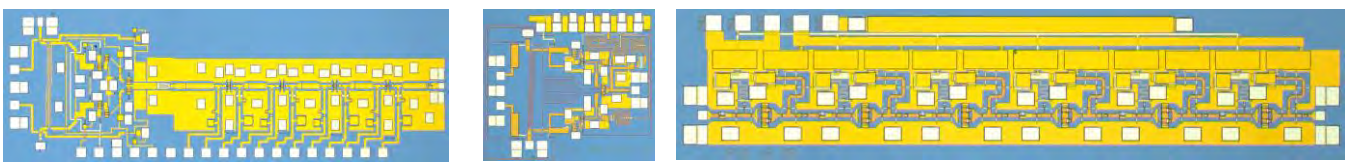
1. Introduction

Emerging mm-wave applications such as e.g. 5G/6G wireless communication and RF sensing (short-range radar sensors) may require compact, low-cost and power efficient electronic beam-steering systems (active phased arrays). This abstract provides an RF performance summary (overview) of different E/W-band front-end MMICs realised in a 60 nm GaN-on-Silicon process. The presented circuit designs and experimental results were obtained within the H2020 project SERENA (2018-2021). The maximum power handling capabilities of GaN-on-Si high electron mobility transistors (HEMTs) are typically below that of GaN-on-Silicon Carbide (GaN-on-SiC) devices but silicon substrates are less expensive and commonly used around the world. GaN-on-Si processes may use wafer sizes up to at least 6-8 inches and this can potentially enable a lower manufacturing cost. Furthermore, to obtain a higher level of integration is a key driver for many emerging mm-wave applications (5G/6G and short-range high resolution radar systems) that could benefit from compact active phased array antennas with adequate performance in terms of high output power and sensitivity over a wide bandwidth. As a result, it can be more cost- and power-efficient to use the same GaN process for mm-wave transmit and receive modules (potentially single-chip). Below, we summarise results of different 60 nm GaN-on-Si E/W-band MMICs; i.e. a single-chip receiver (LNA/down-converter), up-converter and driver.

2. 60 nm GaN-on-Silicon based E/W-Band Front-End MMICs

Figure 1 a-c) show micrographs of some E/W-band MMICs realised in a 60 nm GaN-on-Si process from the foundry OMMIC [1-3]. The substrate thickness used (100 µm) allows cost-effective processing compatible with 6-8 inch wafers and grounded co-planar waveguides are used to suppress undesired higher-order transmission modes. A 4-stage E/W-band LNA design is combined with a frequency down-converter (mixer and doubler) in a single-chip heterodyne W-band receiver (see Fig. 1a). The LNA contains four cascaded common source stages and the transistor gate width is 2×22 µm in all stages to provide a high gain and low NF over a wide bandwidth. The single-chip receiver also includes a down-converter circuit design which is based on a balanced resistive mixer and two frequency doublers that increases the applied local oscillator (LO) frequency by two times. Due to the frequency doubling (from LO/2) the two branches in the down-converter circuit will be 180° out of phase. The differential intermediate frequencies (IF) are provided via high impedance connections at the sources of the two transistors in the mixer sub-circuit. A W-band frequency up-converter circuit design was also realised in the same 60 nm GaN-on-Si process (see Fig. 1b) and it consists of a single-balanced up-conversion mixer with integrated frequency doublers for generating differential LO signals. The IF and the LO signals are applied at the gate terminals of the two transistors in the mixer sub-circuit. The single-ended output (RF) signal is extracted from the drain terminals of those two transistors.

Figure 1c shows a micrograph of a six-stage E/W-band medium power amplifier (MPA) fabricated in the same 60 nm GaN-on-Si process and a transistor gate width of 4×35 µm is used in all stages. The input and output matching networks used in all the stages are fairly simple to minimize circuit area and provide sufficient gain and output power in the target frequency band (~75-100 GHz).



a) b) c)

Figure 1. Micrographs of E/W-band front-end MMICs fabricated in a 60 nm GaN-on-Si process: a) single-chip receiver (LNA and down-converter with frequency doubler), b) up-converter with frequency doubler and c) driver amplifier [1-3].

3. Summary of Results

The characterisation of the fabricated 60 nm GaN-on-Si front-end MMICs was done with RF probes connected to a network analyzer and/or a spectrum analyzer for s-parameters and noise figure/large-signal measurements, respectively. The single-chip receiver (LNA and down-converter) and MPA circuits were assembled in test fixtures with off-chip decoupling capacitors and the DC connections to the chip provided using bond-wires. The measured RF performance of the indicated 60 nm GaN-on-Si front-end MMICs are summarised in Tables 1-2 [1-3]. The LNA sub-circuit used in the single-chip receiver was measured separately and it has a measured small-signal gain in the range of 15-23 dB at 70-95 GHz (V_d=10 V, I_d=70 mA). The measured NF of this LNA design is equal to 4.4-5.5 dB at 90-95 GHz when I_d is 70 mA and it is 2-3 dB higher when I_d=110 mA. This LNA circuit has a measured output referred 1 dB compression point (P_{1dB}) of 9 dBm and 13 dBm at 90-95 GHz when V_d=10 V and I_d was 55 mA and 110 mA, respectively (measured input P_{1dB} is between -10 dBm and 0 dBm at 90-95 GHz). A re-optimised LNA design fabricated in a second 60 nm GaN-on-Si wafer run resulted in a slightly lower measured gain at 70-90 GHz and some dBs higher measured gain above 90 GHz (18 dB at 74 GHz and 19 dB at 95 GHz) when V_d=10 V, I_d=30 mA. Furthermore, the measured NF of the re-designed LNA is 2.5-4.7 dB/3.0-5.0 dB at 75-95 GHz when V_d=10 V, I_d=30/60 mA. The measured output P_{1dB} of this LNA circuit is 3-10 dBm and 7-12 dBm at 75-95 GHz when using those DC bias points [1].

Compared with a 75-80 GHz GaN-on-SiC single-chip receiver (IF=0.1 GHz, CG≤11 dB, input P_{1dB}=-14 dBm, area=5 mm^2) [4], our 60 nm GaN-on-Si single-chip receiver has a higher linearity, wider RF/IF bandwidths and smaller area. The receiver noise figure can be reduced using an improved LNA circuit with a measured average NF of 3.6-4.0 dB at 75-95 GHz [1].
The 60 nm GaN-on-Si up-converter has the lowest conversion loss and smallest chip area among GaN mixers at E/W-band [2].

Table 1. RF performance of 60 nm GaN-on-Si E/W-band front-ends MMICs (LNA/down-converter and up-converter) [1-2].

Circuit	**RF (GHz)**	**IF (GHz)**	**Conv. Gain (dB)**	**P_{1dB} (dBm)**	**Area (mm^2)**
Receiver (LNA/Down-converter)	75-91	1-6	0-7 (IF=5 GHz) 0-6 (IF=2 GHz)	-12 @ 80 GHz (input) -9 @ 91 GHz (input)	4
Up-converter	87.5-95.5	0.1-4.1	-9.5 to -6.5	-8.5 (output)	2

Table 2 shows the experimental results of a 60 nm GaN-on-Si six-stage MPA (or driver amplifier) and such amplifiers also require small circuit areas to reduce the size of single-chip front-ends. The transmitter and receiver circuits should be minimised to enable compact E/W-band single-chip transceiver front-ends. The GaN-on-Si 6-stage driver demonstrates a highly attractive combination of small size together with a relatively high measured gain and output power over a wide bandwidth. The measured output power levels of this 60 nm GaN-on-Si MPA (15-17 dBm at 80-90 GHz) are consistent with the expected requirements of a final stage power amplifier made in this process that has a measured P_{out} of 28 dBm and gain of 14 dB at 89 GHz (the driver amplifier should then deliver near 14 dBm of output power) [3].

Table 2. RF performance of a 60 nm GaN-on-Si E/W-band medium power amplifier [3].

Circuit	**RF (GHz)**	**S_{21} (dB)**	**Power Gain (dB)**	**P_{out} (dBm)**	**Area (mm^2)**
Medium power amplifier (MPA)	77.5-100	14-25	8-16	10.9-17.2	2

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References

[1]. R. Malmqvist, R. Jonsson, A. Bernland, M. Bao, R. LeBlanc, K. Buisman, C. Fager, and K. Andersson, "A W-band single-chip receiver in a 60 nm GaN-on-Silicon foundry process," in Proc. EuMIC'2021, April 2022, pp. 51-54.

[2]. M. Bao, R. Malmqvist, R. Jonsson, J. Hansryd, and K. Andersson, "A W-band up-conversion mixer with integrated LO frequency doublers in a 60 nm GaN technology," in Proc. EuMIC'2021, April 2022, pp. 108-111.

[3]. R. Malmqvist, R. Jonsson, M. Bao, R. LeBlanc, and K. Andersson, "Compact high-gain driver amplifier MMICs for 60 nm GaN-on-Si W-band single-chip transceivers," in Proc. EuMIC'2022, Sept. 2022, pp. 95-98.

[4]. I. Kallfass, R. Quay, H. Massler, S. Wagner, D. Schwantuschke, C. Haupt, R. Kiefer, and O. Ambacher,, "A single-chip 77 GHz heterodyne receiver MMIC in 100 nm AlGaN/GaN HEMT technology," in Proc. IMS'2011, 2011, pp. 1-4.